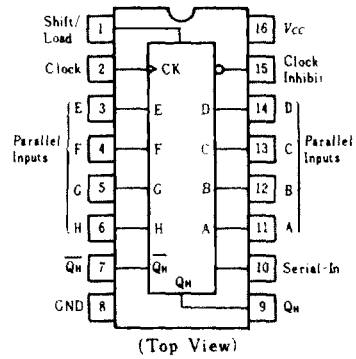
HD74HC165 ● Parallel-load 8-bit Shift Register

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the Shift/Load input. Also included is a gated clock input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

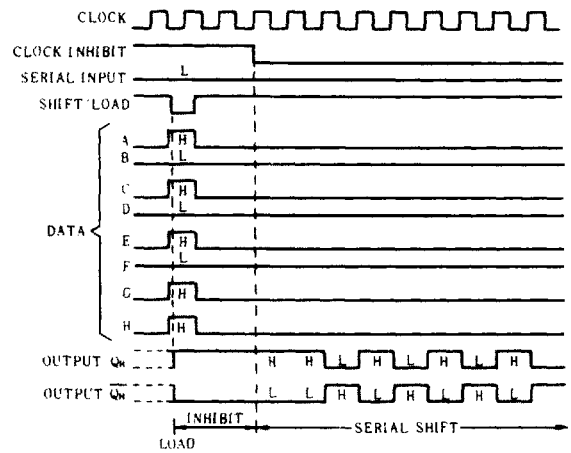
■ PIN ARRANGEMENT



■ FEATURES

- High Speed Operation: t_{pd} (Clock to Q_H)=21ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)=4μA max. (Ta=25°C)

■ TIMING DIAGRAM



■ FUNCTION TABLE

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A……H	Q_A	Q_B	Q_H
L	X	X	X	a……h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	typ	max	Ta=−40~+85°C min	max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	T_a=25°C min	T_a=25°C typ	T_a=25°C max	T_a=−40~+85°C min	T_a=−40~+85°C max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	27	—	21	
		6.0		—	—	32	—	25	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	Clock to Q_H or $\overline{Q_H}$	—	—	150	—	190	ns
		4.5		—	21	30	—	38	
		6.0		—	—	26	—	33	
		2.0	Shift/Load to Q_H or $\overline{Q_H}$	—	—	160	—	200	
		4.5		—	23	32	—	40	
		6.0		—	—	27	—	34	
		2.0	H to Q_H or $\overline{Q_H}$	—	—	150	—	190	
		4.5		—	21	30	—	38	
		6.0		—	—	26	—	33	
Setup Time	t_{su}	2.0	Parallel Data Inputs to Shift/Load	100	—	—	125	—	ns
		4.5		20	−3	—	25	—	
		6.0		17	—	—	21	—	
		2.0	Serial Input to Clock	100	—	—	125	—	
		4.5		20	3	—	25	—	
		6.0		17	—	—	21	—	
		2.0	Shift/Load to Clock	100	—	—	125	—	
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
Removal Time	t_{rem}	2.0	Clock to Clock Inhibit or Clock Inhibit to Clock	100	—	—	125	—	ns
		4.5		20	6	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	Shift/Load to Parallel Data Input	5	—	—	5	—	ns
		4.5		5	−3	—	5	—	
		6.0		5	—	—	5	—	
		2.0	Clock to Serial Data Input	5	—	—	5	—	
		4.5		5	3	—	5	—	
		6.0		5	—	—	5	—	
		2.0	Clock to Shift/Load	5	—	—	5	—	
		4.5		5	—	—	5	—	
		6.0		5	—	—	5	—	
Pulse Width	t_w	2.0	Clock, Shift/Load	80	—	—	100	—	ns
		4.5		16	6	—	20	—	
		6.0		14	—	—	17	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF