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# HD74HC299

8-bit Universal Shift/Storage Register (with 3-state outputs)

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## Description

The HD74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and 3-state feature, this device is ideally suited for interfacing with bus lines in a bus oriented system. Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines  $S_0$  and  $S_1$  high. This places the 3-state outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding clear input is provided to clear the register whether the outputs are enabled or disabled.

## Features

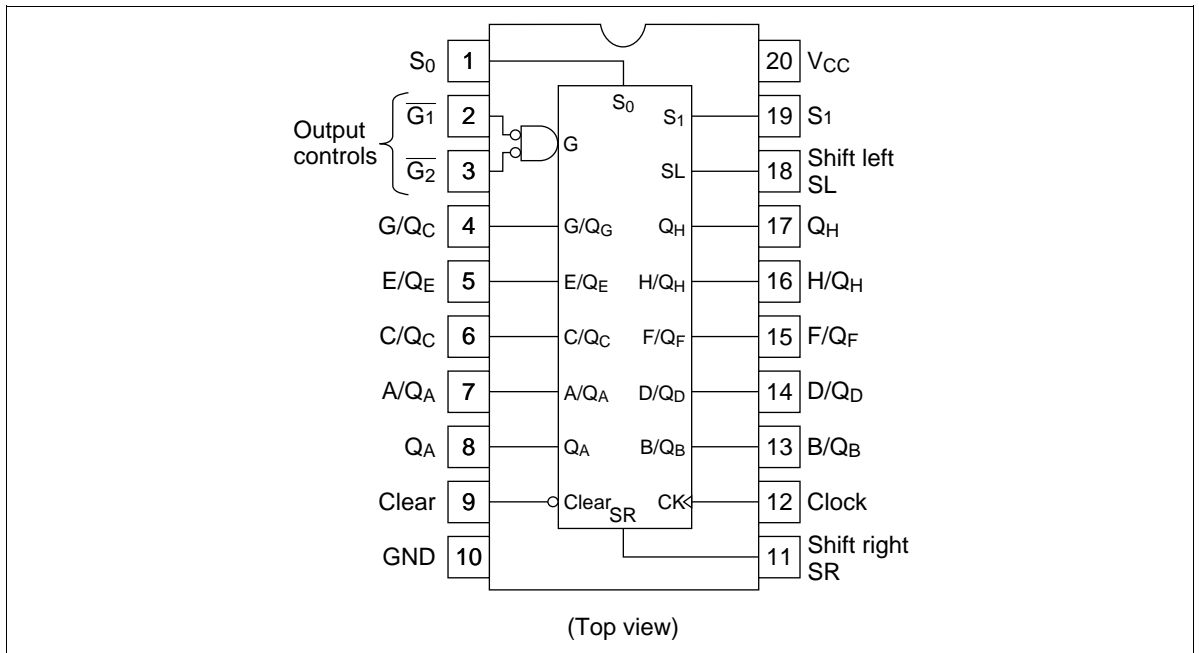
- High Speed Operation
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

## Function Table

		Inputs					Serial Inputs/Outputs										Outputs		
		Clear	Function Select		Output Control		Clock	S <sub>L</sub>	S <sub>R</sub>	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>	
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>	
Shift	H	L	H	L	L		X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>	
Right	H	L	H	L	L		X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>	
Shift	H	H	L	L	L		H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H	
Left	H	H	L	L	L		L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L	
Load	H	H	H	X	X		X	X	a	b	c	d	e	f	g	h	a	h	

- Notes:
1. a to h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.
  2. Q<sub>A0</sub> to Q<sub>H0</sub>; the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.
  3. Q<sub>An</sub> to Q<sub>Hn</sub>; the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the most-recent transition of the clock.
  4. † = ; When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.
  5. When clear is low, outputs of Q<sub>A</sub>' and Q<sub>H</sub>' are low, in spite of other inputs.

Pin Arrangement

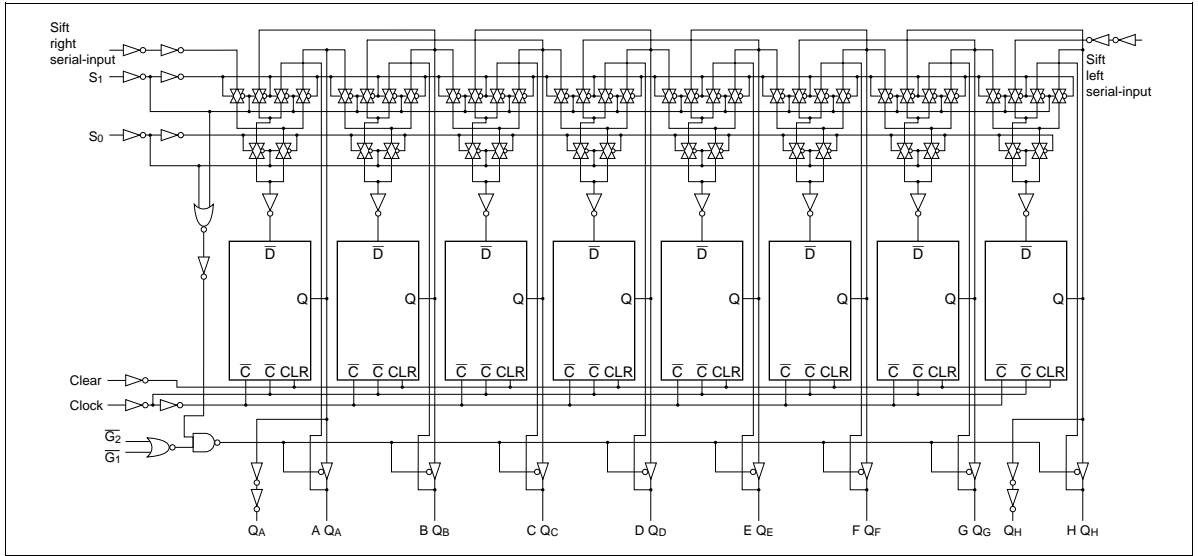


Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to +7.0	V
Input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Output current	$I_{OUT}$	$\pm 35$	mA
DC current drain per $V_{CC}$ , GND	$I_{CC}$ , $I_{GND}$	$\pm 75$	mA
DC input diode current	$I_{IK}$	$\pm 20$	mA
DC output diode current	$I_{OK}$	$\pm 20$	mA
Power dissipation per package	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}C$

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## Block Diagram



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DC Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min			Max	
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			Q <sub>A</sub> ' & Q <sub>H</sub> ' I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			Outputs I <sub>OH</sub> = -5.2 mA
		4.5	4.18	—	—	4.13	—			A/Q <sub>A</sub> thru I <sub>OH</sub> = -6 mA
	V <sub>OL</sub>	6.0	5.68	—	—	5.63	—	H/Q <sub>H</sub> Outputs I <sub>OH</sub> = -7.8 mA		
		2.0	—	0.0	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			Q <sub>A</sub> ' & Q <sub>H</sub> ' I <sub>OH</sub> = 4 mA
		6.0	—	—	0.26	—	0.33			Outputs I <sub>OH</sub> = 5.2 mA
		4.5	—	—	0.26	—	0.33			A/Q <sub>A</sub> thru I <sub>OH</sub> = 6 mA
		6.0	—	—	0.26	—	0.33			H/Q <sub>H</sub> Outputs I <sub>OH</sub> = 7.8 mA
Off-state output current	I <sub>OZ</sub>	6.0	—	—	±0.5	—	±5.0			μA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA	

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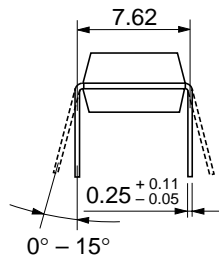
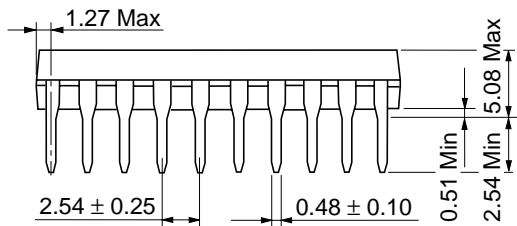
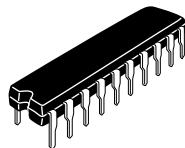
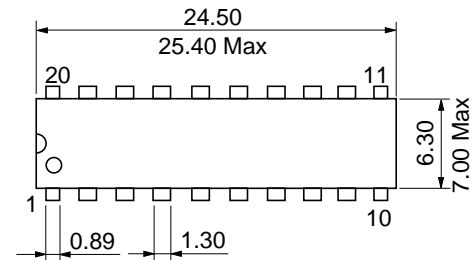
## AC Characteristics ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Maximum clock frequency	$f_{max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	23		
Propagation delay time	$t_{PLH}$	2.0	—	—	190	—	240	ns	Clock to $Q_A'$ or $Q_H'$
		4.5	—	—	38	—	48		
		6.0	—	—	32	—	41		
	$t_{PHL}$	2.0	—	—	220	—	275	ns	Clear to $Q_A'$ or $Q_H'$
		4.5	—	—	44	—	55		
		6.0	—	—	37	—	47		
	$t_{PLH}$	2.0	—	—	190	—	240	ns	Clock to $Q_A - Q_H$
		4.5	—	—	38	—	48		
		6.0	—	—	32	—	41		
	$t_{PHL}$	2.0	—	—	220	—	275	ns	Clear to $Q_A - Q_H$
		4.5	—	—	44	—	55		
		6.0	—	—	37	—	47		
Output enable time	$t_{ZH}$	2.0	—	—	160	—	200	ns	
		4.5	—	—	32	—	40		
		6.0	—	—	27	—	34		
Output disable time	$t_{LZ}$	2.0	—	—	160	—	200	ns	
		4.5	—	—	32	—	40		
		6.0	—	—	27	—	34		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Select
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time	$t_h$	2.0	5	—	—	5	—	ns	Select
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Removal time	$t_{rem}$	2.0	50	—	—	65	—	ns	Clear
		4.5	10	—	—	13	—		
		6.0	9	—	—	11	—		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		

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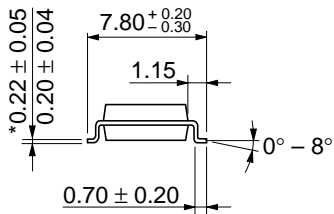
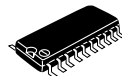
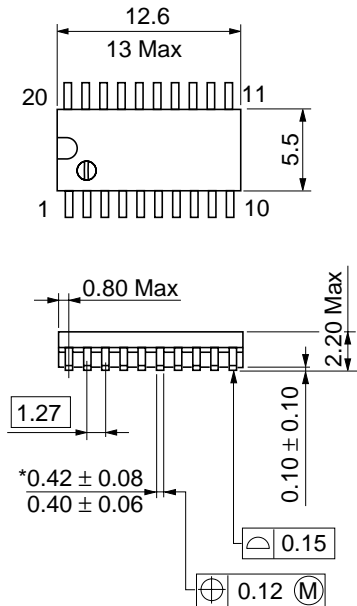
AC Characteristics ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns) (cont)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Output rise/fall time	$t_{TLH}$	2.0	—	—	60	—	75	ns	A/Q <sub>A</sub> thru H/Q <sub>H</sub> outputs
		4.5	—	—	12	—	15		
		6.0	—	—	10	—	13		
	$t_{THL}$	2.0	—	—	75	—	95	ns	Q <sub>A</sub> ' & Q <sub>H</sub> ' outputs
		4.5	—	—	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C <sub>in</sub>	—	—	5	10	—	10	pF	



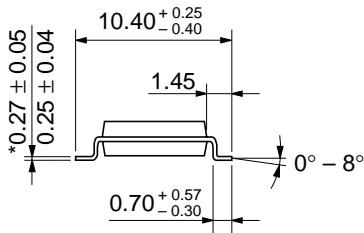
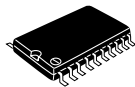
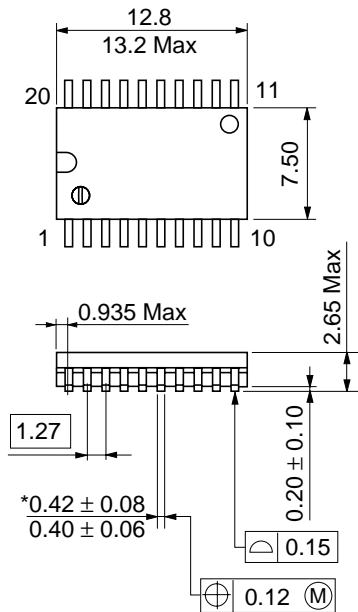
Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

\*Dimension including the plating thickness  
 Base material dimension

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